

FIG. 1
BACKGROUND ART

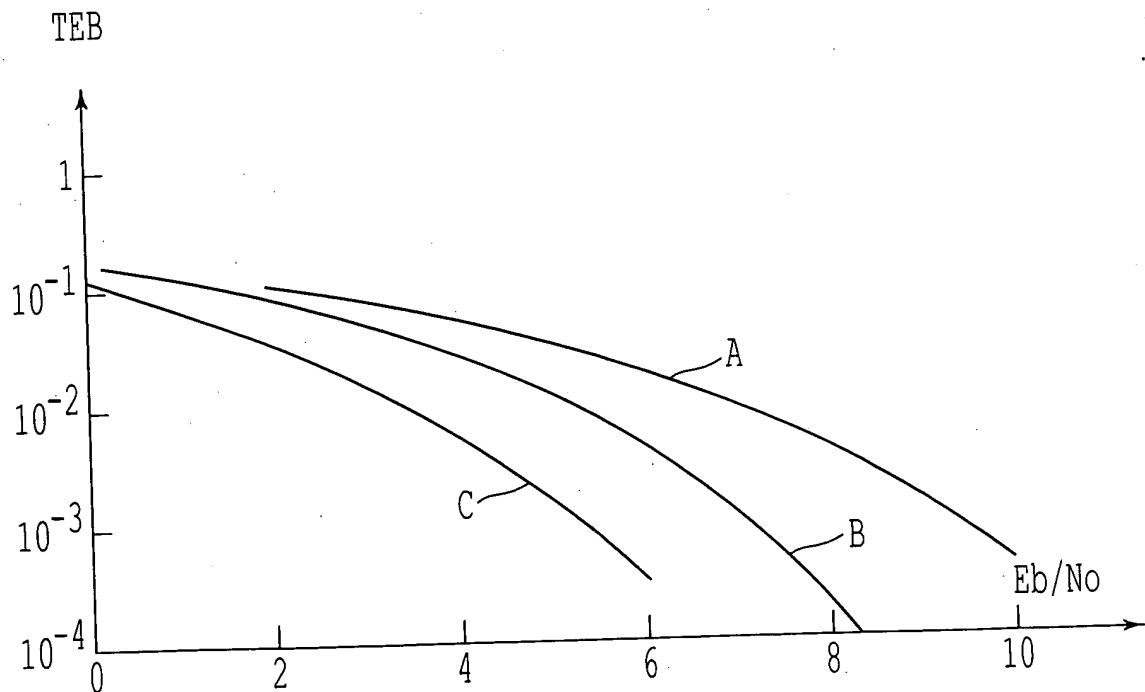


FIG. 8

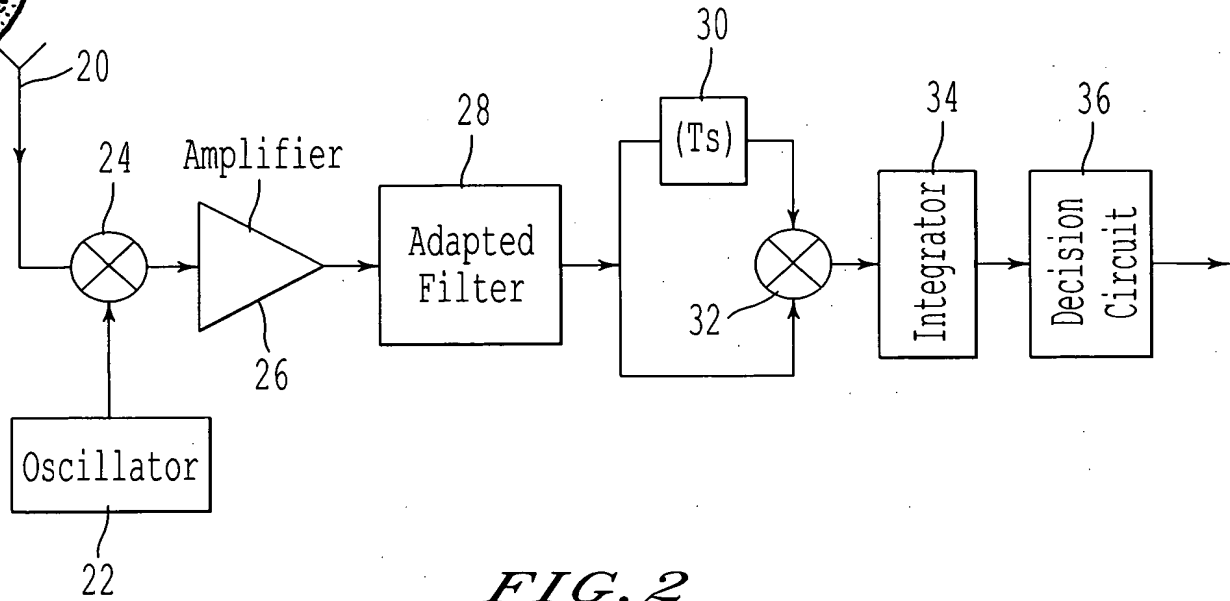
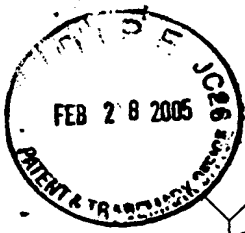


FIG. 2
BACKGROUND ART

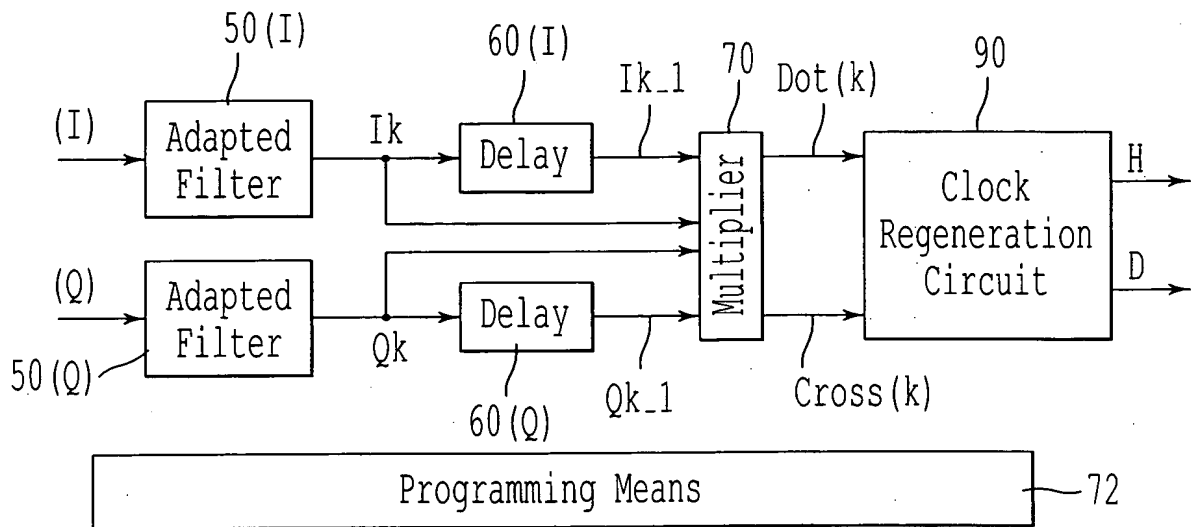
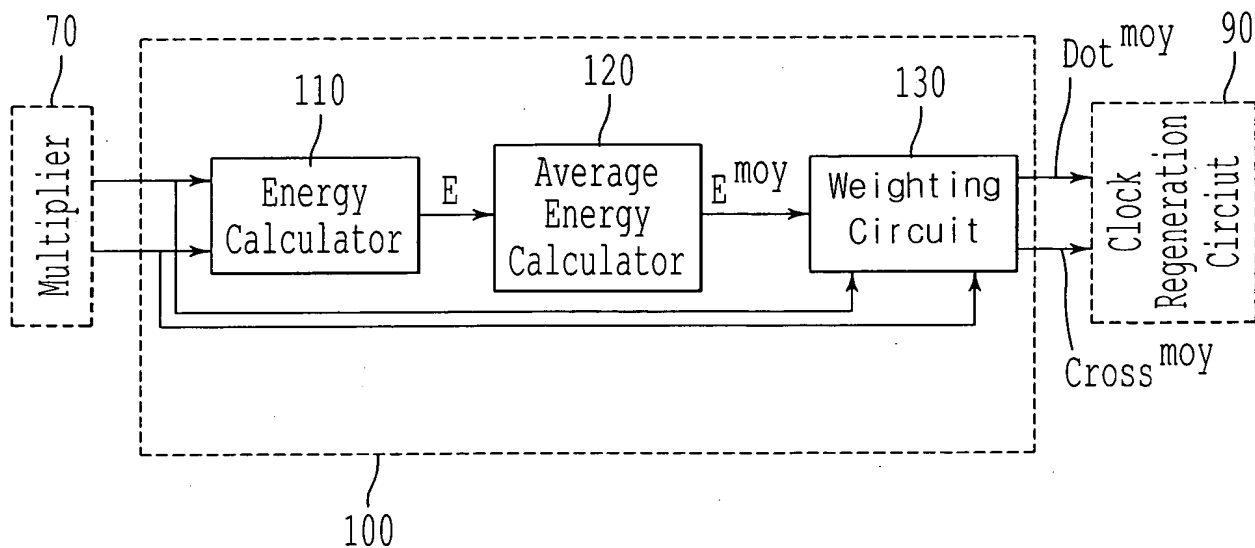
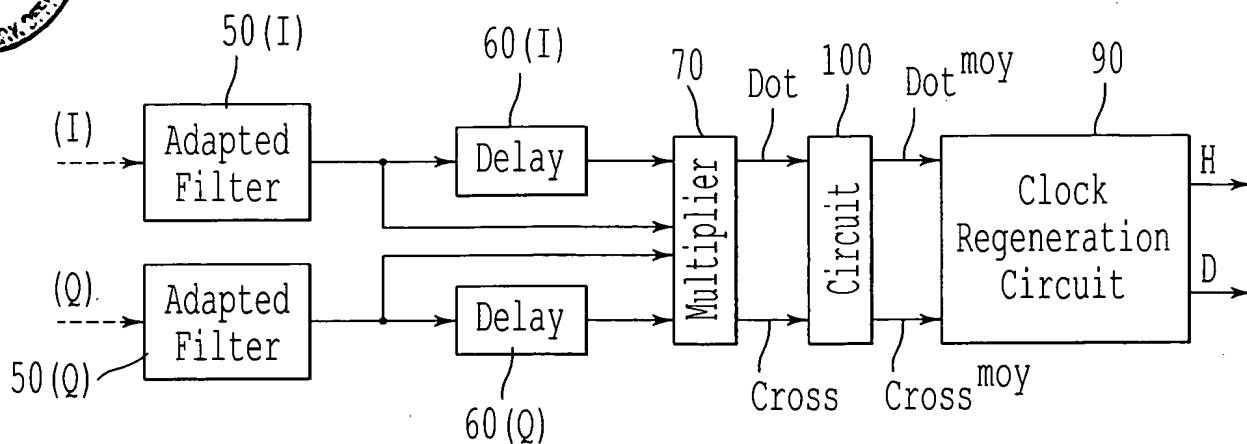


FIG. 3
BACKGROUND ART



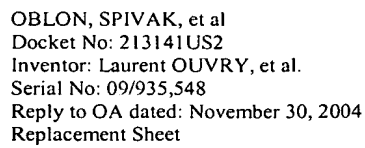


FIG. 6

Block diagram of a multi-channel receiver system (FIG. 6). The system includes a common input line **E** at the bottom. Four parallel processing channels are shown:

- Channel 1: **Filter 201**, **Power Calculator 211**, and **Channel Selector 230**.
- Channel 2: **Filter 202**, **Power Calculator 212**, and **Channel Selector 230**.
- Channel 3: **Filter 203**, **Power Calculator 213**, and **Channel Selector 230**.
- Channel 4: **Filter 20M** (dashed), **Power Calculator 21M** (dashed), and **Channel Selector 232** (dashed).

The **Channel Selector 230** outputs to a **MOK Decoder 250**. The **Channel Selector 232** outputs to a **Demux 240**. The **Demux 240** outputs to a **Differential Demux 260**. The **Differential Demux 260** outputs to a **Decoder 270**. The **Decoder 270** outputs to a **Circuit 280**, which is connected to an output **OS**. The **Circuit 280** also receives inputs **m MOK** and **m DP** from the **MOK Decoder 250** and the **Decoder 270** respectively.

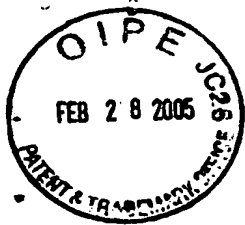


FIG. 7

